



**SANDISK® 3-D OTP MEMORY  
NAND INTERFACE  
512 BYTE PAGE  
128MBIT TO 1GBIT**

**DATA SHEET**

DOCUMENT NUMBER: **DS034**  
REVISION: **1.1**  
REVISION DATE: 09-07-06

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**1.0 REVISION HISTORY**

REVISION	HISTORY	REV. DATE	REMARK
0.8	Initial Release	6/30/05	Trinity Family Initial Release
0.81	Update	07/06/05	Slight modification
1.00	Production Release	12/19/05	Deepsleep Function Included, Archive Storage Spec Updated, Part Numbers Updated
1.1	Reformatting	09/07/06	Reformatted to SanDisk look and feel (logos, copyright, etc.); changed numbering; updated operating and storage temp specs; omitted part numbering; by Nivita Verma

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## 2.0 PIN DESCRIPTION

### 2.1 PIN PLACEMENT



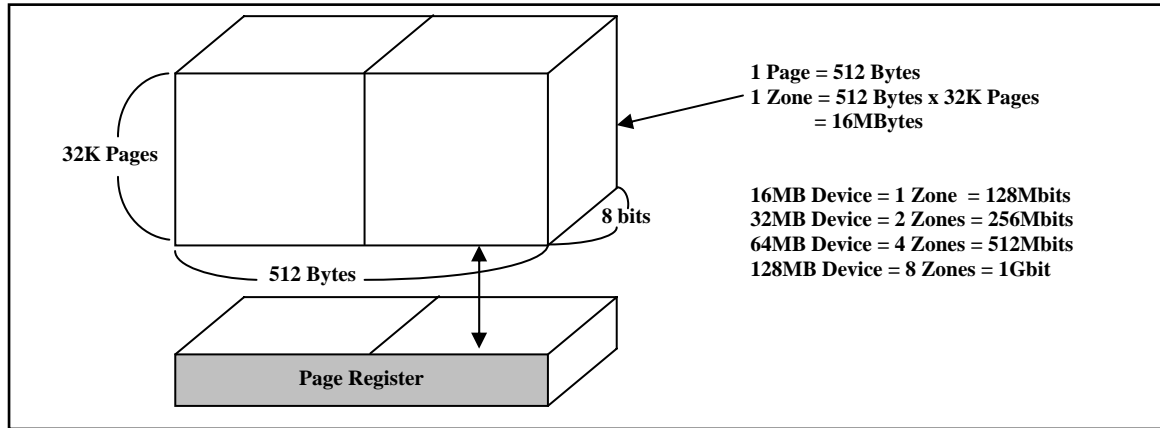
### 2.2 SANDISK® 3-D OTP MEMORY PIN MAP

PIN		PIN		PIN		PIN	
1	NC	9	GND	17	NC	25	GND
2	DS	10	NC	18	NC	26	V <sub>DD</sub>
3	R/B#	11	NC	19	NC	27	IO <sub>5</sub>
4	NC	12	CLE	20	IO <sub>1</sub>	28	IO <sub>6</sub>
5	RE#	13	ALE	21	IO <sub>2</sub>	29	IO <sub>7</sub>
6	CE#	14	WE#	22	IO <sub>3</sub>	30	IO <sub>8</sub>
7	NC	15	WP#	23	IO <sub>4</sub>	31	NC
8	V <sub>DD</sub>	16	NC	24	NC	32	NC

## 2.3 DETAILED PIN DESCRIPTION

PIN NAME	PIN FUNCTION	DETAILED PIN DESCRIPTION
IO <sub>1</sub> - IO <sub>8</sub>	Data Input/Outputs	Handles the input and output of addresses, commands, and data.
CE#	Chip Enable	Acts as the device selection signal. When set to 'H' in the read state, the standby mode is assumed. In the Busy state during the execution of write operations (R/B# = L), both 'H' and 'L' are accepted. (Standby will not be assumed when 'H')
CLE	Command Latch Enable	Enables commands to be sent to the internal command register of the device. Setting the level to 'H' when the WE# signal falls and rises causes the data on the I/O terminals to be written into the command register
ALE	Address Latch Enable	Controls whether data is sent to the internal address register or the internal data register in the device. By setting the level to 'H' when the WE# signal falls and rises, the data present at the I/O terminals is written into the address register as address data. By setting the level to 'L' when the WE# signal falls and rises, the data present at the I/O terminals is written into the data register as input data
RE#	Read Enable	Enables the output of data serially from the I/O terminals. From the time RE# falls, valid output data will be present at the I/O terminals after t <sub>REA</sub> , and the internal column address counter advances (+1)
WE#	Write Enable	Used to write data present at the I/O terminals into the device
WP#	Write Protect	Prohibits writing. At 'L', the operation of the internal high voltage generating circuit is reset. Normally, the system is operated with this signal 'H', but if the power supply signals are irregular (ON/OFF, etc.), this signal should be 'L' in order to protect stored data from unexpected operations. In the event that the V <sub>DD</sub> voltage is outside the range in which correct operation is assured, it is recommended that the level be set to 'L'
R/B#	Ready/Busy Output	Serves as open drain output that indicates the internal operating conditions of the device. During write and read operations, Busy (R/B# L) is output. Ready is automatically output when the operation is finished. R/B# is attached to a 12Kohm internal pull-up.
DS	Deep Sleep	Enables low power "sleep" state to conserve battery life.
GND	Ground Input	Ground
V <sub>DD</sub>	Power Supply	Power Supply Voltage

**3.0 ARRAY ORGANIZATION**







**4.0 OPERATING COMMAND REQUIREMENTS**

Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Data is latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle. The 64Mbyte physical space requires 26 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Write need the same four address cycles following the required command input. Device operations are selected by writing specific commands into the command register. The following table defines the specific commands of the SanDisk 3DM chip.

COMMAND	OP CYCLE	VALID DURING BUSY
Serial Data Input	80 h	N
Read1	00 h	N
Read2	01 h	N
Reset	FF h	Y
Page Write	10 h	N
Status Read	70 h	Y
ID Read	90 h	N

## 5.0 OPERATION MODES AND COMMAND TABLES

### 5.1 OPERATING MODES

MODE	CLE	ALE	CE#	WE#	RE#	WP#
Command Input	H	L	L		H	X
Address Input	L	H	L		H	X
Data Input	L	L	L		H	X
Data Output	L	L	L	H		X
While writing	X	X	X	X	X	H
Write Protect	X	X	X	X	X	L

H:  $V_{IH}$  L:  $V_{IL}$  X =  $V_{IH}$  or  $V_{IL}$

### 5.2 READ MODES

COMMAND	1 <sup>ST</sup> CYCLE	POINTER
Read1	00 h	0 to 255
Read2	01 h	256 to 511

### 5.3 VALID READ OPERATING MODES

MODE	CLE	ALE	CE#	WE#	RE#	D <sub>1</sub> – D <sub>8</sub>	STATUS
Read Mode	L	L	L	H	L	D <sub>OUT</sub>	Active
Output Deselect	L	L	L	H	H	Z	Active
Standby	L	L	H	H	X	Z	Standby

### 5.4 DEVICE CODES

MEMORY SIZE	DEVICE CODE
128Mbit	73h
256Mbit	75h
512Mbit	76h
1Gbit	79h

**5.5 STATUS REGISTER OUTPUTS**

PIN	STATUS	“0”	“1”
IO <sub>1</sub>	Pass or Fail (only valid if IO <sub>7</sub> = “1”)	Pass	Write Failure: Failed repair during Write
IO <sub>2</sub>	Reserved	Default	--
IO <sub>3</sub>	Reserved	Default	--
IO <sub>4</sub>	Reserved	Default	--
IO <sub>5</sub>	Reserved	Default	--
IO <sub>6</sub>	Reserved	Default	--
IO <sub>7</sub>	Ready or Busy	Busy	Ready
IO <sub>8</sub>	Write Protect	Protected	Not Protected

**5.6 PERFORMANCE SPECIFICATIONS**

SYMBOL	PARAMETER	MIN	TYPICAL	MAX
t <sub>PROG</sub>	Write time	-	350 us*	8 ms**
t <sub>R</sub>	Data transfer time	-	140 us	300 us
t <sub>RSTread</sub>	Device reset time (read cycle)	-	2 us	10 us
t <sub>RSTwrite</sub>	Device reset time (write cycle)	-	2 us	10 us

\*t<sub>PROG typ</sub> is defined as 50% 0 data pattern at 3.3V and 25C operating temperature.

\*\*t<sub>PROG max</sub> may occur during rare redundancy self-repair operation.

## 5.7 AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	MIN	MAX	SYMBOL	PARAMETER	MIN	MAX
t <sub>CYCLE</sub>	Cycle time	50 ns	--	T <sub>RR</sub>	Ready to RE# low	20 ns	--
t <sub>CLS</sub>	CLE setup to WE#	0 ns	--	t <sub>REAI</sub> D	RE# access time (ID read)	--	35 ns
t <sub>CLH</sub>	CLE hold to WE#	10 ns	--	t <sub>RHZ</sub>	RE# high to output high impedance	--	30 ns
t <sub>CS</sub>	CE# setup to WE#	0 ns	--	t <sub>REH</sub>	RE# high hold time	15 ns	--
t <sub>CH</sub>	CE# hold to WE#	10 ns	--	t <sub>IR</sub>	Output high impedance to RE# low	0 ns	--
t <sub>WP</sub>	WE# pulse width	25 ns	--	t <sub>RSTO</sub>	RE# access time (status read)	--	35 ns
t <sub>ALS</sub>	ALE setup to WE#	0 ns	--	t <sub>CSTO</sub>	CE# access time (status read)	--	45 ns
t <sub>ALH</sub>	ALE hold WE#	10 ns	--	t <sub>WHR</sub>	WE# high to RE# low	30 ns	--
t <sub>DS</sub>	Data setup to WE#	20 ns	--	t <sub>WHC</sub>	WE# high to CE# low	30 ns	--
t <sub>DH</sub>	Data hold to WE#	10 ns	--	t <sub>AR1</sub>	ALE low to RE# low (Add. Reg. & ID read)	100 ns	--
t <sub>WC</sub>	Write cycle time	50 ns	--	t <sub>CR</sub>	CE# low to RE# low (Data Reg. & ID read)	100 ns	--
t <sub>WH</sub>	WE# high hold time	15 ns	--	t <sub>WB</sub>	WE# high to busy	--	100 ns
t <sub>RP</sub>	Read pulse width	35 ns	--	t <sub>AR2</sub>	ALE low to RE# low (read cycle)	50 ns	--
t <sub>REA</sub>	RE# access time (serial data)	--	35 ns	t <sub>CRY</sub>	CE# high to ready: R = (V <sub>DDmax</sub> - V <sub>OLmax</sub> ) / (I <sub>OL</sub> + I <sub>L</sub> )	--	10 us
t <sub>WW</sub>	WP# high to WE# low	100 ns	--	t <sub>CHZ</sub>	CE# high to output high impedance	--	20 ns
t <sub>DS_POR</sub>	DS asserted after V <sub>dd</sub> established	100us	--	t <sub>DS_WU</sub>	DS low to CLE high	100us	--

**5.8 OPERATING ENVIRONMENT**
**5.8.1 DC REQUIREMENTS**

SYMBOL	PARAMETER	MIN	MAX
V <sub>DD</sub>	Supply voltage	2.7 V	3.6 V
V <sub>IH</sub>	Input high voltage	2.2 V	V <sub>DD</sub> + 0.3 V
V <sub>IL</sub>	Input low voltage	-0.3 V	0.6 V
V <sub>OH</sub>	Output high voltage (I <sub>OH</sub> = -400uA)	2.4 V	-
V <sub>OL</sub>	Output low voltage (I <sub>OL</sub> = 2.1mA)	-	0.4 V
I <sub>CC1</sub> *	Read current (typ)	20 mA	
I <sub>CC2</sub>	Read current (max)	30 mA	
I <sub>CC3</sub> *	Write current (typ)	40 mA	
I <sub>CC4</sub>	Write current (max)	80 mA	
I <sub>CC5</sub>	Standby current	100 uA	
I <sub>CCDS</sub>	Deep Sleep current	15uA	
I <sub>LI</sub>	Input Leakage	±10 uA	
I <sub>LO</sub>	Output Leakage	±10 uA	

\* Typical values measured at room temperature and 3.3V.

**5.8.2 ABSOLUTE MAXIMUM RATING**

SYMBOL	PARAMETER	MIN	MAX
V <sub>DD</sub>	Supply Voltage		4.6 V
V <sub>IH</sub>	Input high voltage	--	V <sub>DD</sub> +0.3 ≤ 4.6V
V <sub>IL</sub>	Input low voltage	-0.3 V	--

**5.8.3 CAPACITANCE**

SYMBOL	PARAMETER	MIN	MAX
C <sub>L</sub>	Capacitance due to input or output pin	10 pF	15 pF

**5.8.4 STORAGE CONDITION**

SYMBOL	PARAMETER	MIN	MAX
T <sub>store</sub>	Storage Temperature Requirements	-40°C	150 °C

**5.8.5 LIFETIME AND DATA RETENTION**

SYMBOL	PARAMETER	MIN	MAX
L <sub>dr</sub> *	Data Retention Lifetime	100 Years	-
L <sub>shelf</sub> *	Shelf Lifetime	100 Years	

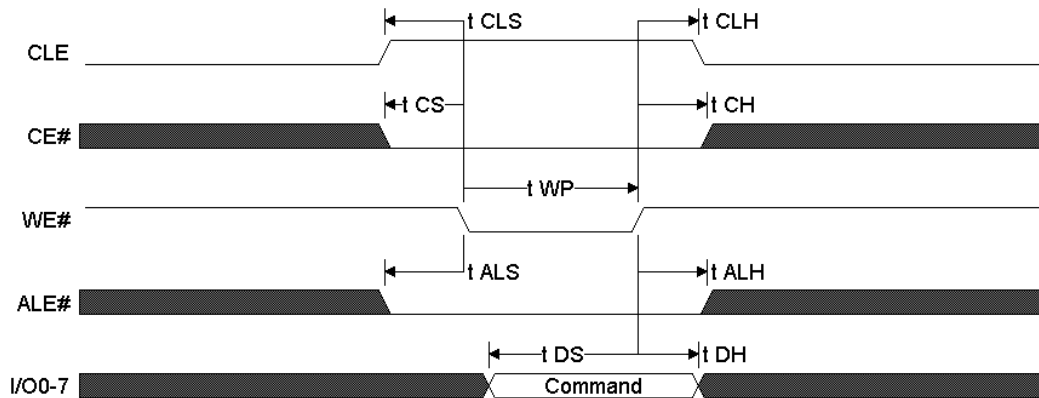
\*Shelf and Data Retention lifetime are specified with an average temperature of 25°C ± 10°C and <40% relative humidity

5.8.6 OPERATING TEMPERATURE

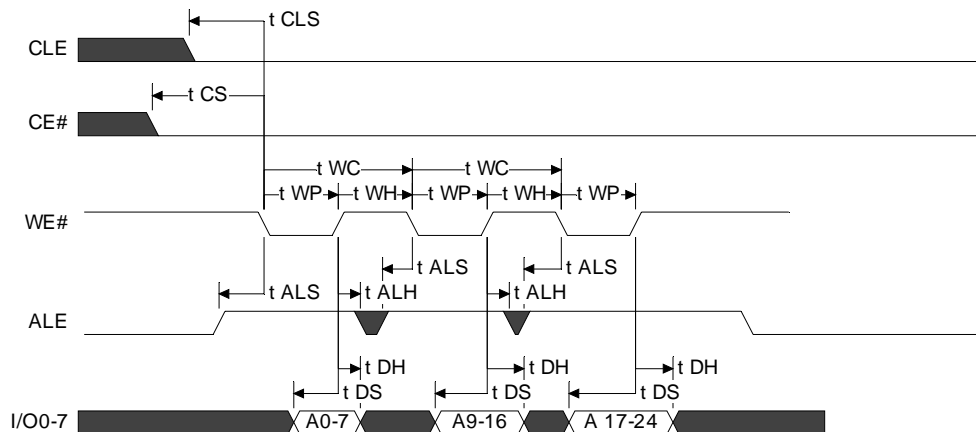
SYMBOL	PARAMETER	MIN	MAX
Toper	Operational Temperature Requirements	-25°C	85°C

6.0 TIMING SPECIFICATION

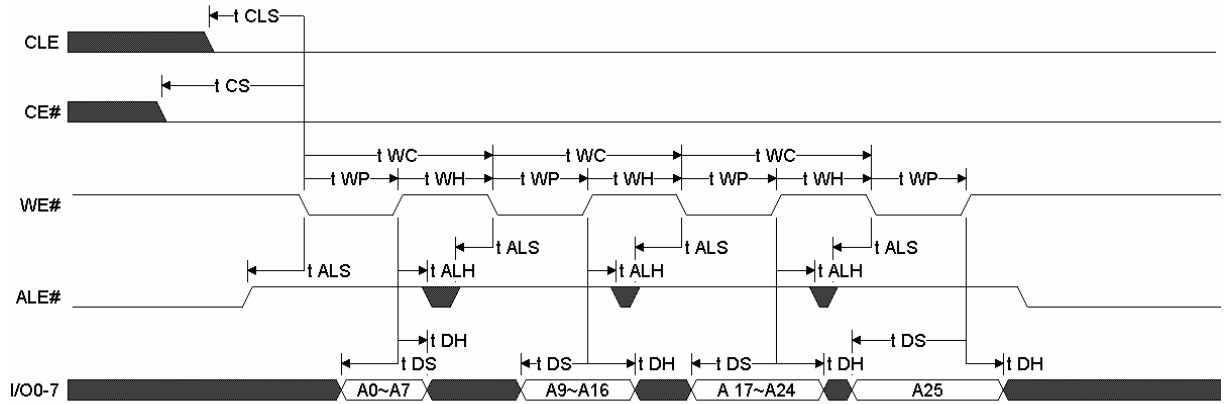
6.1 COMMAND LATCH CYCLE



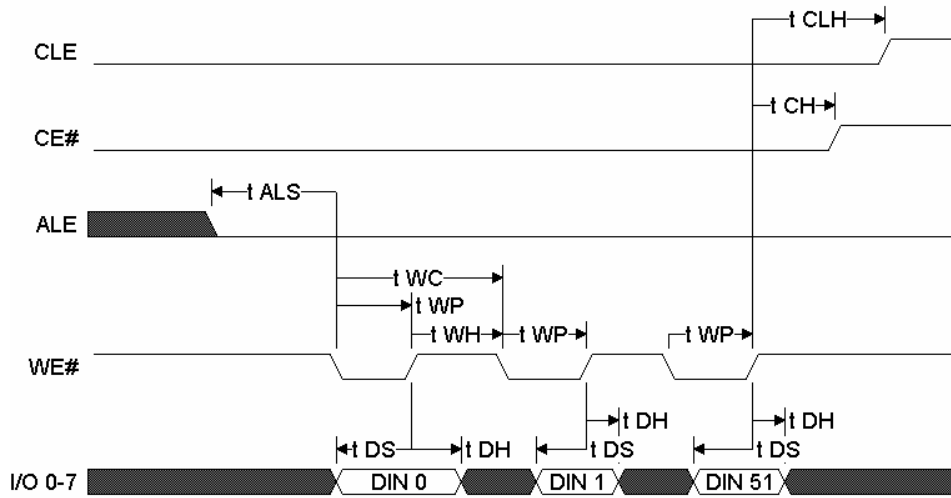
6.2 ADDRESS LATCH CYCLE  
(Address Cycle for 128Mb and 256Mb)



(Address Cycle for 512Mb)



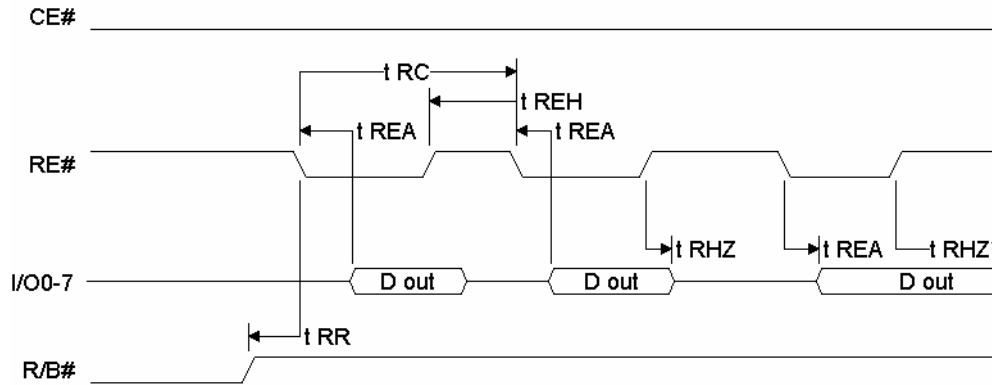
6.3 INPUT DATA LATCH CYCLE



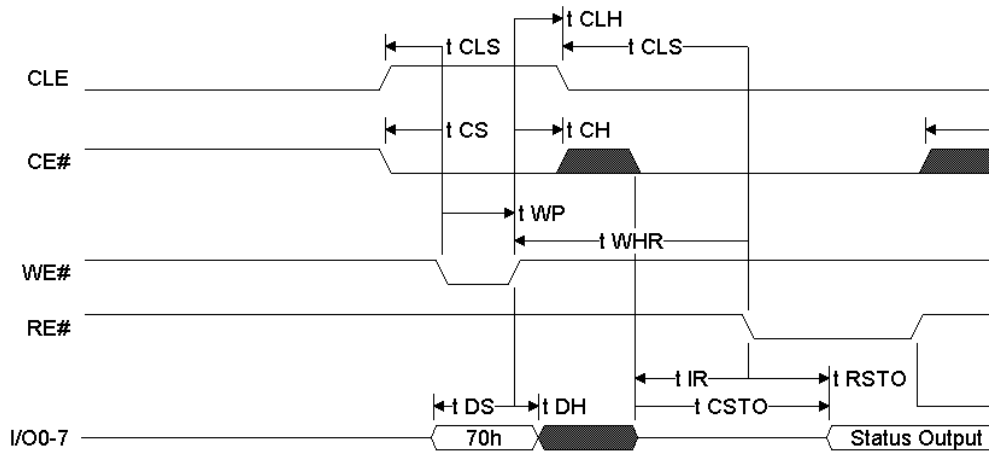
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6.4 SEQUENTIAL OUT CYCLE AFTER READ

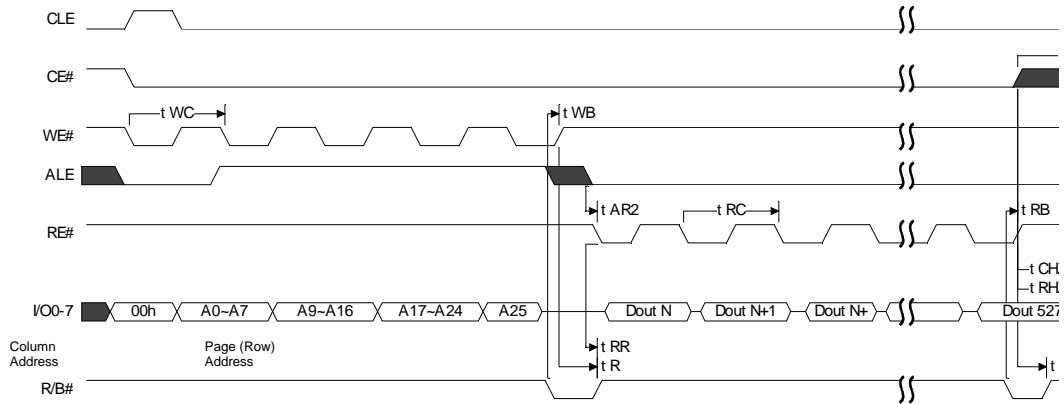
(CLE = L, WE# = H, ALE = H)



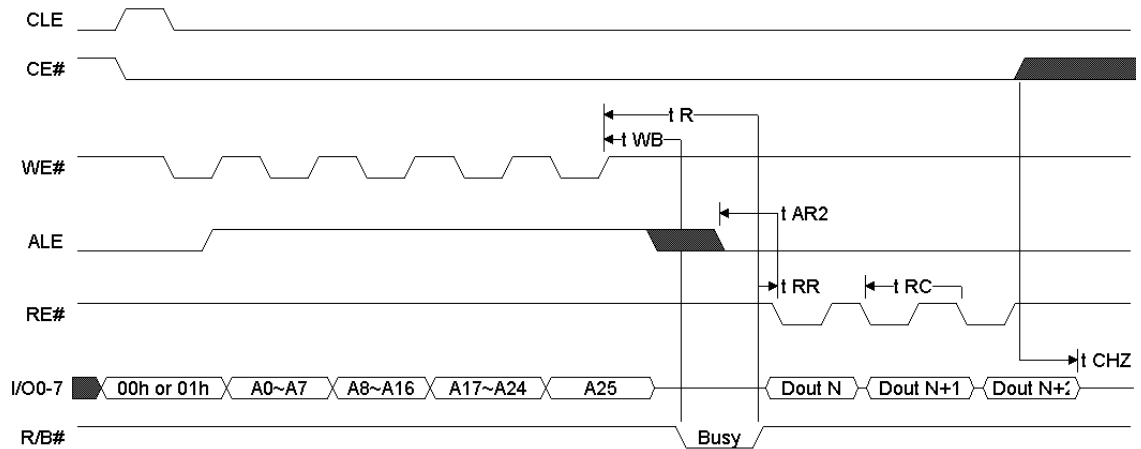
6.5 STATUS READ CYCLE



6.6 READ1 AND READ2 OPERATIONS (READ ONE PAGE)

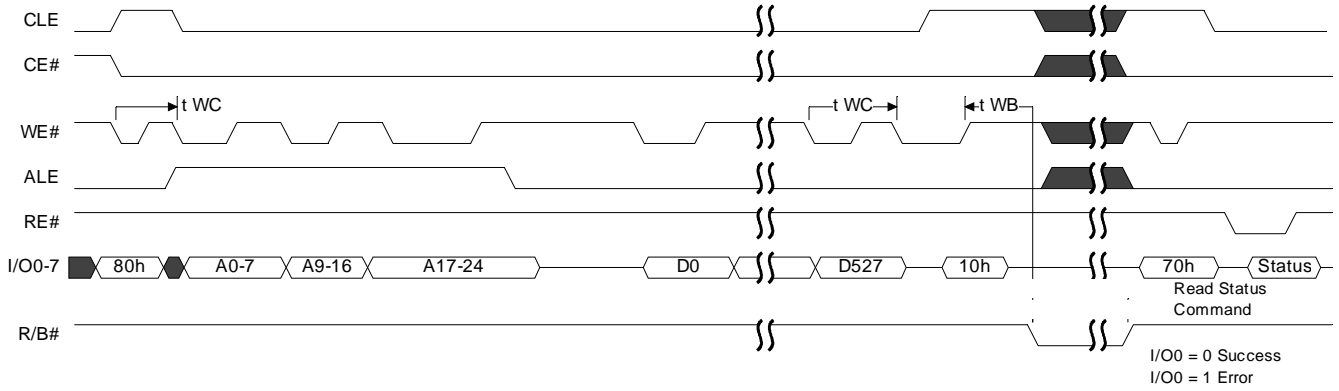


6.7 READ1 AND READ2 OPERATIONS (INTERCEPTED BY CE#)

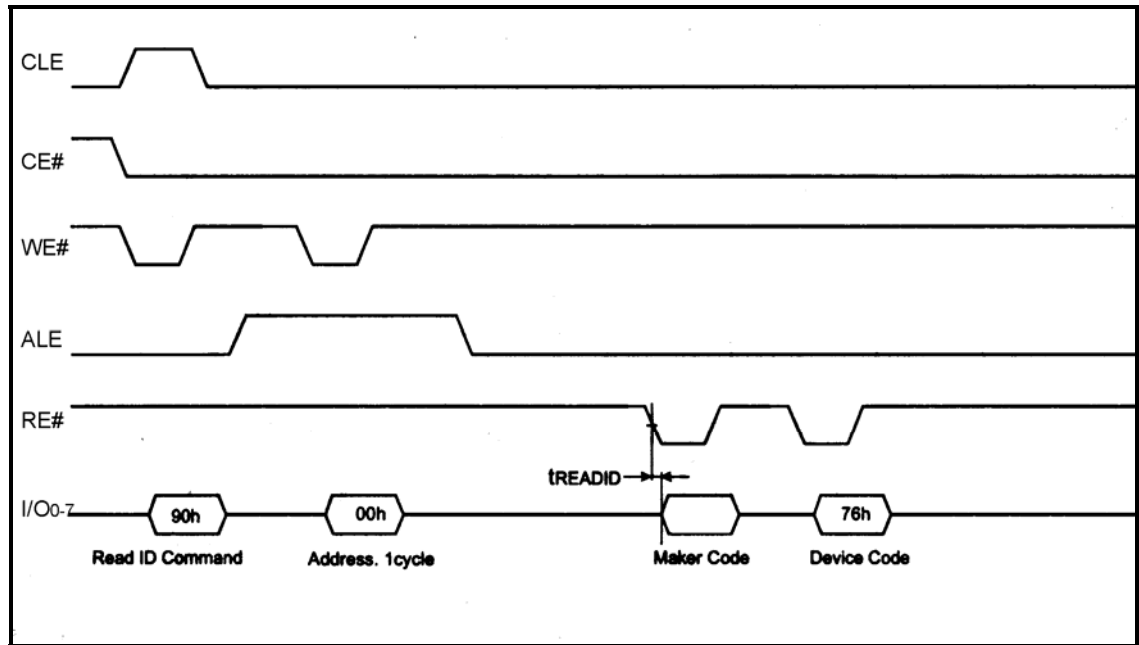


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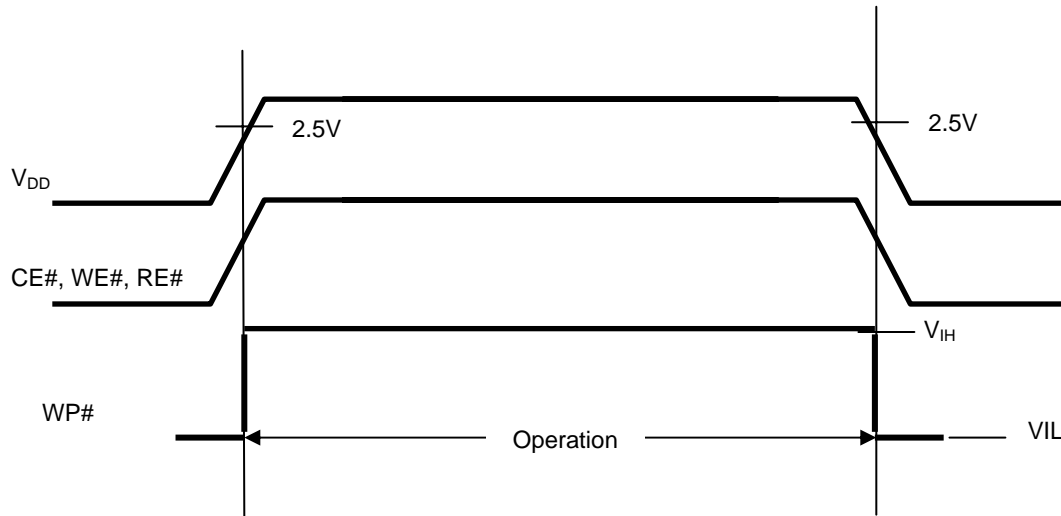
**6.8 PAGE WRITE OPERATION**



**6.9 MANUFACTURE & DEVICE ID READ OPERATION**



6.10 POWER ON REQUIREMENTS

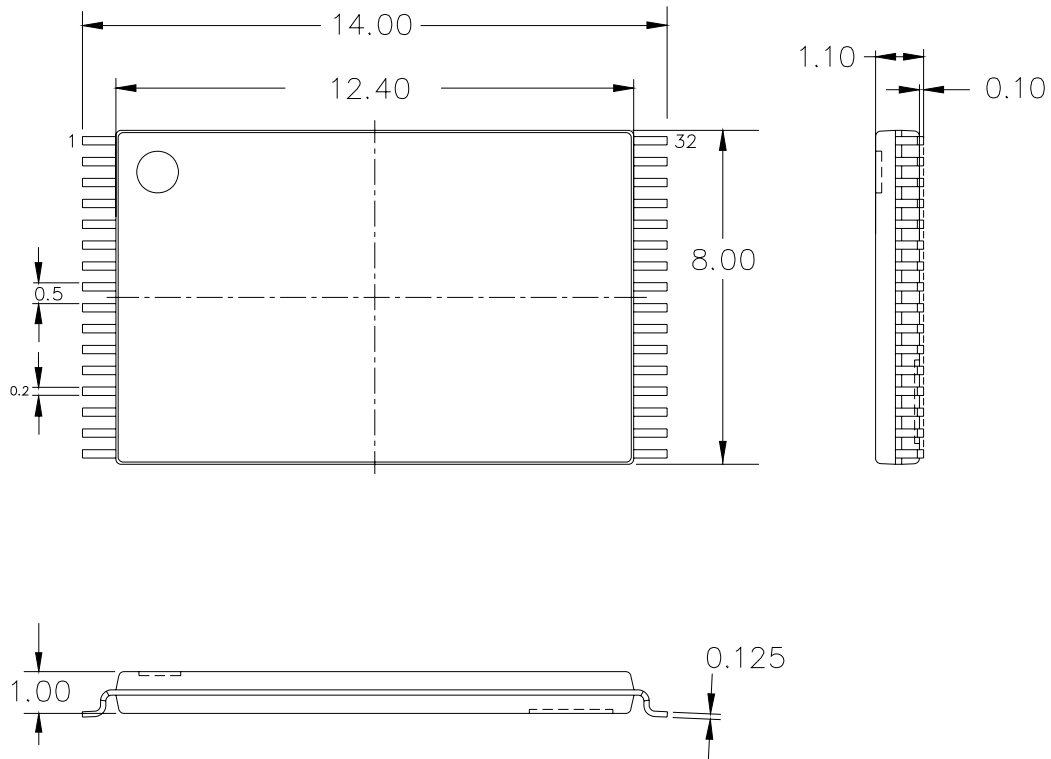


To ensure proper startup a RESET command should be entered after V<sub>DD</sub> has been established.

7.0 READ/BUSY# LOAD REQUIREMENTS

The Ready/Busy# signal has an internal 12Kohm pull-up attached to it, thereby removing the requirement for an external pull-up on the system PCB. Attaching an external pull-up will not damage the part in any way, but is not necessary for proper functionality.

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**8.0 32-PIN TSOP PACKAGE DIMENSIONS***Notes:*

- All dimensions listed are nominal values listed in mm.
- Alternative packages may be available upon request.